Code No: V0423 **R07** SET - 1

II B. Tech II Semester, Supplementary Examinations, April - 2012

SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
******0*******

1. a) Find the octal equivalent of $(2F.C4)_{16}$ and the hex-equivalent of $(762.013)_8$. (8M)
   b) What do you understand by the l's and 2's complements of a binary number? What will be the range of decimal numbers that can be represented using a 16-bit 2's complement format? (8M)

2. a) What is meant by expanded POS and minimal POS? Obtain expanded POS and minimal POS expression for the following logic expression $f(A,B,C) = A\overline{B} + \overline{A}B$
   b) Simplify using Boolean-algebra
      i) $AB + A\overline{B}C + \overline{A}B\overline{C} + B\overline{C}$
      ii) $AB + A\overline{C} + C + AD + A\overline{B}C + AB$ (8M+8M)

3. Simplify the following expressions using k-map and implement with NOR gate?
   $f(A,B,C,D) = \pi M\,(0,2,4,6,7,8,10,12,13,15)$
   $f(A,B,C,D) = \Sigma m\,(0,1,4,5,6,7,9,11,15) + \Sigma_{\phi}(10,14)$ (16M)

4. a) Design a circuit to convert Excess-3 code to BCD code using 4:16 de-multiplexer.
   b) Explain the functionality of priority encoder with its logic diagram? (8M+8M)

5. a) Design a BCD to excess3 code converter using PLA logic, Draw its truth table and logic diagram. (10M)
   b) Given a switching function f(x1, x2, x3) = (0,1,3) determine whether or not it is realizable by a single threshold element, and if it is, find appropriate weights and threshold. (6M)

6. a) What is the Q output logic status of following input conditions of the J-K flip-flop hiving active HIGH J and K inputs and active LOW PRESET and CLEAR inputs,?
      i) J = 1, K = 0,PRESET=1,CLEAR = 1;
      ii) J = 1, K = 1,PRESET=0,CLEAR = 1;
      iii) J = 0, K = 1,PRESET=1,CLEAR = 0;
      iv) J = K = 0, PRESET = 0, CLEAR = 1.
   b) Draw the logic diagram of a 4 bit binary ripple counter using negative edge triggering. (8M+8M)

7. a) State the capabilities and limitations of finite state machine? (6M)
   b) Find the Equivalence partition for the given Machine. Show a standard form of the corresponding reduced machine. (10M)

PS	NS, Z	
	X=0	X=1
A	B,1	H,1
B	F, 1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. Design the ASM chart, Data path circuit & Control circuit to implement traditional division of two four bit binary numbers. (16M)

Code No: V0423 **R07** SET - 2

II B. Tech II Semester, Supplementary Examinations, April - 2012

SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any **FIVE** Questions
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*******0******

1. a) Do the following conversions:
   i) Eight-bit 2's complement representation of $(-23)_{10}$;
   ii) Decimal equivalent of $(00010111)_2$ represented in 2's complement form. (8M)
   b) Write:
   i) Hamming (7,4) code for 0000 using even parity
   ii) Hamming (11,7) code for 1111111 using odd parity. (8M)

2. a) What is meant by expanded SOP and minimal SOP? Obtain expanded SOP and minimal SOP expression for the following logic expression. $f(A,B,C) = A(B+\overline{C})$ (8M)
   b) Simplify using Boolean-algebra
   i) $AB + A(B+C) + \overline{B}(B+D)$
   ii) $\overline{B}\,\overline{C}\,D + \overline{(B+C+D)} + \overline{B}\,\overline{C}\,\overline{D}\,E$ (8M)

3. Obtain the minimal expression using the tabulation method?
   $f(A,B,C,D) = \Sigma m(1,5,6,12,13,14) + d(2,4)$ (16M)

4. a) Discuss how does a priority encoder differ from a conventional encoder explain with the help of a truth table and logic diagram? (6M)
   b) Design a circuit to convert Excess-3 code to BCD code using 4:16 de-multiplexer. (10M)

5. a) Discuss the advantages of PLD's in comparison with fixed logic device? (6M)
   b) Design a BCD to excess3 code converter using PLA logic, Draw its truth table and logic diagram. (10M)

6. a) Draw the logic diagram of a JK flip-flop and using excitation table, explain its operation.
   b) Draw the block diagram of a 4-bit serial adder and explain its operation. (8M+8M)

7. a) Explain the procedure to minimize completely specified sequential machine? (6M)
   b) Find the Equivalence partition for the given Machine. Show a standard form of the corresponding reduced machine. (10M)

PS	NS, Z	
	X=0	X=1
A	B,1	H,1
B	F, 1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. a) Explain the control subsystem implementation of weighting machine? (8M)
   b) Draw the state diagram of a Mod-6 counter and convert it into the ASM chart. Explain the sequence of operation in each ASM block. (8M)

Code No: V0423 **R07** SET - 3

II B. Tech II Semester, Supplementary Examinations, April - 2012

SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communications Engineering)

Time: 3 hours Max Marks: 80

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
*******0******

1. a) Add −118 and −32 firstly using eight-bit 2's complement arithmetic and then using16-bit 2's complement arithmetic. Comment on the results. (8M)
   b) Write:
   i) Hamming (7,4) code for 0000 using even parity
   ii) Hamming (11,7) code for 1111111 using odd parity. (8M)

2. a) Discuss different types minimal and expanded forms of Boolean expressions? Illustrate with examples. (8M)
   b) Simplify using Boolean-algebra.
   i) $AB + A(B + C) + \overline{B}(B + D)$
   ii) $\overline{B}\,\overline{C}\,D + \overline{(B + C + D} + \overline{B}\,\overline{C}\,\overline{D}\,E$ (8M)

3. Obtain the minimal expression using the tabulation method?
   $f(A,B,C,D) = \Sigma m(1,5,6,12,13,14) + d(2,4)$ (16M)

4. a) Implement a full subtractor combinational circuit using a 3-to-8 decoder and external NOR gates. (8M)
   b) Design a 32-to-1 multiplexer using 8-to-1 multiplexers having an active LOW ENABLE input and a 2-to-4 decoder? (8M)

5. a) What is meant by programming in PLD's. Give the hardware procedure of programming in PROM's and EPROM's. (8M)
   b) Show the logic arrangement of both a PROM and a PLA required to implement a binary full adder. (8M)

6. a) What is the Q output logic status of following input conditions of the J-K flip-flop hiving active HIGH J and K inputs and active LOW PRESET and CLEAR inputs,?
   i) J = 1, K = 0, PRESET=1, CLEAR = 1;
   ii) J = 1, K = 1, PRESET=0, CLEAR = 1;
   iii) J = 0, K = 1, PRESET=1, CLEAR = 0;
   iv) J = K = 0, PRESET = 0, CLEAR = 1. (8M)
   b) Design Modulo-6 counter using T flip-flops. (8M)

7. a) Distinguish between Mealy and Moore machines (6M)
   b) Find the Equivalence partition for the given Machine. Show a standard form of the corresponding reduced machine. (10M)

PS	NS, Z	
	X=0	X=1
A	B,1	H,1
B	F, 1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

8. The state diagram of a control is shown in the following figure 1.
   i) Determine the equivalent ASM chart
   ii) Design the control unit using D flip-flops and decoder (16M)

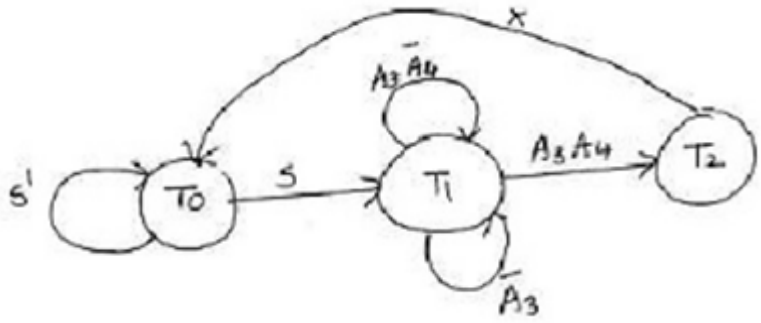

Figure 1

Code No: V0423 **R07** SET - 4

II B. Tech II Semester, Supplementary Examinations, April - 2012

SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours Max Marks: 80

Answer any **FIVE** Questions
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1. a)Subtract using 2's complement arithmetic.
   i) $(-64)_{10}$ from $(+32)_{10}$
   ii) $(29.A)_{16}$ from $(4F.B)_{16}$. (8M)
   b) Give the difference between the cyclic and non cyclic codes explain with the help of example? (8M)

2. a) Discuss different types minimal and expanded forms of Boolean expressions? Illustrate with examples. (8M)
   b) Obtain expanded POS , minimal POS expression and expanded SOP, minimal SOP expression for the following logic expressions.
   i) $f(A,B,C)=A\overline{B}+\overline{A}B$
   ii) $f(A,B,C)=A(B+\overline{C})$ (8M)

3. Simplify the following expressions using k-map and implement with NOR gate?
   $f(A,B,C,D)=\pi M\ (0,2,4,6,7,8,10,12,13,15)$
   $f(A,B,C,D)=\Sigma m\ (0,1,4,5,6,7,9,11,15)+\Sigma_{\phi}(10,14)$ (16M)

4. a) What is a de-multiplexer and how does it differ from a decoder? How can a decoder be used as a de-multiplexer? (8M)
   b) Implement a full adder combinational circuit using a 3-to-8 decoder and external NOR gates. (8M)

5. a) What is meant by programming in PLD's. Give the hardware procedure of programming in PROM's and EPROM's. (8M)
   b) A and B are two binary variables. The objective is to design a magnitude comparator to produce A = B, A<B and A>B outputs. Design a suitable PLD with a PAL (8M)

6. a) What is a clocked J-K flip-flop? Explain with the help of truth tables what improvement does it have over a clocked R-S flip-flop? (8M)
   b) Design a sequence detector which detects 110101? Implement the sequence detector by using D-type flip-flop? (8M)

7. a) How the incompletely specified state machine is simplified? (8M)
   b) Find the Equivalence partition for the given Machine. Show a standard form of the corresponding reduced machine. (8M)

PS	NS, Z	
	X=0	X=1
A	D,0	H,1
B	F, 1	C,1
C	D,0	F,1
D	C,0	E,1
E	C,1	D,1
F	D,1	D,1

8. The state diagram of a control is shown in the following Figure 1.
   i) Determine the equivalent ASM chart
   ii) Design the control unit using multiplexers (16M)

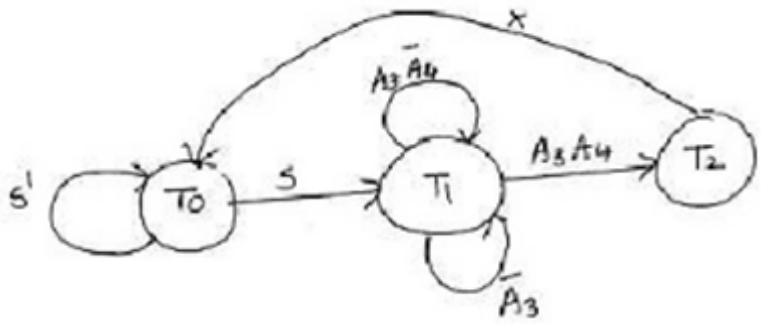

Figure 1